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- 1 1. A system comprising:
2 a digital signal processor comprising a bus connectable to a
3 memory; and
4 a butterfly coprocessor connected to the bus, wherein the butterfly
5 coprocessor performs an operation scheduled by the digital signal processor.
- 1 2. The system of claim 1, wherein the digital signal processor further
2 comprises:
3 a data address generator coupled to the bus, wherein the data
4 address generator addresses the memory on behalf of a requesting device.
- 1 3. The system of claim 2, wherein the digital signal processor further
2 comprises an arithmetic unit for performing arithmetic operations in the digital
3 signal processor.
- 1 4. The system of claim 3, wherein the arithmetic unit further
2 comprises a branch metric unit for performing branch metric calculations.
- 1 5. The system of claim 4, wherein the arithmetic unit further
2 comprises one or more registers to which the branch metric unit may store one
3 or more results.
- 1 6. The system of claim 5, wherein the data address register may
2 address one or more registers in the arithmetic unit.
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1 7. The system of claim 1, wherein the butterfly coprocessor further
2 includes a plurality of butterfly units for performing butterfly operations.

1 8. The system of claim 7, wherein the butterfly operations are parallel
2 operations.

1 9. The system of claim 8, wherein the plurality of butterfly units in the
2 butterfly coprocessor further perform add-compare-select operations at the
3 direction of the digital signal processor.

1 10. The system of claim 8, wherein the plurality of butterfly units in the
2 butterfly coprocessor further perform approximations of log sum exponential
3 operations at the direction of the digital signal processor.

1 11. The system of claim 8, wherein a path metric retrieved from a path
metric memory is accessed by the data address generator of the digital signal
processor.

1 12. The system of claim 11, wherein the data address generator of the
digital signal processor further retrieves a branch metric from the branch metric
unit.

1 13. A method comprising:
2 identifying a stage of a trellis diagram;
3 calculating branch metrics for each node of the stage; and

4 simultaneously computing two or more path metrics for the stage
5 based upon the branch metrics.

1 14. The method of claim 13, further comprising:
2 storing the path metrics in a memory.

- 1 15. The method of claim 13, calculating the branch metrics for each
- 2 node of the stage further comprising:
 - 3 identifying a number of nodes in the stage;
 - 4 identifying a number of branches extending from each node; and
 - 5 calculating a branch metric for each branch.

- 1 16. The method of claim 14, simultaneously computing two or more
- 2 path metrics for the stage based upon the branch metrics further comprising:
 - 3 identifying a node of the stage;
 - 4 retrieving a prior path metric from the memory, wherein the prior
 - 5 path metric leads to the node;
 - 6 identifying a number of branches extending from the node in the
 - 7 stage; and
 - 8 allocating a butterfly unit for each branch extending from the
 - 9 node, wherein the butterfly unit calculates a new path metric from the prior path
 - 10 metric and the branch metric.

17. A method comprising:

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2 receiving a request to decode a bit stream, wherein the bit stream
3 was encoded by an encoder and the encoder is described using a trellis diagram;
4 identify a stage of the trellis diagram;
5 compute branch metrics for all nodes of the stage;
6 retrieve path metrics for a different stage of the trellis diagram
7 from a memory; and
8 simultaneously calculate new path metrics for each node of the
9 stage.

18. The method of claim 17, further comprising:
1 storing the new path metrics for each node of the stage in the
2 memory; and
3 identifying a new stage of the trellis diagram.

19. An article comprising a medium storing a software program which,
1 when executed, causes a processor-based system to:
2 identify a stage of a trellis diagram;
3 calculate branch metrics for each node of the stage; and
4 simultaneously compute two or more path metrics for the stage
5 based upon the branch metrics.

20. The article of claim 19, further storing a software program which,
1 when executed, causes a processor-based system to store the path metrics in a
2 memory.

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1 21. A system comprising:
2 a digital signal processor, comprising:
3 a bus connectable to a memory;
4 a data address generator and
5 an arithmetic unit; and
6 a butterfly coprocessor connected to the bus, wherein the butterfly
7 coprocessor performs an operation scheduled by the digital signal processor.
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1 22. The system of claim 21, wherein the digital signal processor further
2 comprises a software program which, upon execution:
3 identifies a stage of a trellis diagram;
4 identifies a number of nodes in the stage; and
5 identifies a number of branches extending from each node.

1 23. The system of claim 22, wherein the butterfly coprocessor further
2 comprises a plurality of butterfly units.

1 24. The system of claim 23, wherein the number of butterfly units
2 equals the number of nodes in the stage.

1 25. The system of claim 24, wherein the operation performed by the
2 butterfly coprocessor comprises computing path metrics for the stage.

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- 1 26. The system of claim 25, wherein the butterfly units simultaneously
- 2 compute a path metric for each node of the stage.

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